REDUNDANCY CIRCUIT FOR MEMORY ARRAY AND METHOD FOR DISABLING NON-REDUNDANT WORDLINES AND FOR ENABLING REDUNDANT WORDLINES

Abstract of the Disclosure

A redundancy circuit for a memory array and a method are provided for disabling non-redundant wordlines and for enabling redundant wordlines. A memory defect address is compared with a current address to be accessed. When there is a miscompare, the access to a non-redundant wordline is allowed to take place as normal. When the memory defect address matches the current address the entire wordline decoder is deactivated through a reset signal and the redundant wordline is activated.